Applicants	Muratov et al.	**COMMUNICATION REGARDING CERTIFICATE OF CORRECTION**
Patent No.	6,919,715	
Issue Date	7/19/2005	
Serial No.	10/668,752	
Attorney Docket No.	125.067US02	
Title: METHODS TO CONTROL THE DROOP WHEN POWERING DUAL MODE PROCESSORS AND ASSOCIATED CIRCUITS		

ATTN: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants hereby request issuance of a Certificate of Correction in U.S. Letters Patent No. 6,919,715 as specified on the attached Certificate (Form PTO/SB/44). Please find enclosed documentation supporting errors identified in the above noted patent, referred to herein as Exhibits A and B.

With respect to the errors identified in the claims of the issued patent, Exhibit A is a copy of pages 1 to 6 of an Amendment and Response (including claims 2 to 7 as allowed; renumbered as claims 1 to 6 in issued patent) and a signed Certificate of Transmission indicating filing of the Response with the U.S. Patent & Trademark Office on February 28, 2005. Exhibit B is a copy of Cols. 13 to 16 of the issued patent. The identified errors constitute typographical errors and as such, do not introduce new matter.

Applicants believe these corrections as specified are necessary due to Office errors and therefore do not believe that any fee is due for requesting a Certificate of Correction for this patent. However, if deemed necessary, the Office is authorized to charge any additional fees found due to Deposit Account No. 502432. Please contact the undersigned if you have any questions.

Respectfully submitted,

Date: December 13, 2007

/David D. Freitag/

David D. Freitag
Reg. No. 56,675

Attorneys for Applicant
Fogg & Powers LLC
P.O. Box 581339
Minneapolis, MN 55458-1339
T – (612) 332-4720
T – (612) 332-4731

EXHIBIT A

Applicant(s)	Muratov	**AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.116 EXPEDITED EXAMINATION PROCEDURE**
Serial No.	10/668,752	
Filing Date	September 23, 2003	
Group Art Unit	2838	
Examiner Name	Younghuie J. Han	
Confirmation No.	1792	
Attorney Docket No.	125.067US02	
Title: METHODS TO CONTROL THE DROOP WHEN POWERING DUAL MODE PROCESSORS AND ASSOCIATED CIRCUITS		

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants have reviewed the Advisory Action mailed February 1, 2005 and the Final Office Action mailed on October 18, 2004. Please amend the above-identified application as follows.

Amendments to the Claims are reflected in the listing of claims that begins on page 2 of this paper.

Remarks begin on page 4 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of claims:

1. (Canceled)

2. (Currently amended) A method of operating a DC/DC converter having an output coupled to a load with two or more modes of operations, the method comprising:

coupling a power source to an input of the DC/DC converter;

creating a droop in an output signal to the load in response in part to a signal from the power source and in response in part to the operating mode of the load such that the droop is substantially symmetrical throughout the operational modes of the DC/DC converter[.]; and ~~The method of claim 1,~~ wherein creating the droop in the output signal further comprises:

multiplying a sensed current in a feedback loop with a signal that is inversely proportional to a frequency of the load.

3. (Currently amended) A method of operating a DC/DC converter having an output coupled to a load with two or more modes of operations, the method comprising:

coupling a power source to an input of the DC/DC converter;

creating a droop in an output signal to the load in response in part to a signal from the power source and in response in part to the operating mode of the load such that the droop is substantially symmetrical throughout the operational modes of the DC/DC converter[.]; and ~~The method of claim 1,~~ wherein creating the droop in the output signal further comprises[:]

multiplying a sensed current in a feedback loop with a signal that is inversely proportional to a reference voltage, wherein the reference voltage is associated with a desired operating voltage of the load.

4. (Currently amended) A method of operating a DC/DC converter having an output coupled to a load with two or more modes of operations, the method comprising:

coupling a power source to an input of the DC/DC converter;

creating a droop in an output signal to the load in response in part to a signal from the power source and in response in part to the operating mode of the load such that the droop is substantially symmetrical throughout the operational modes of the DC/DC converter[.]; and

~~The method of claim 1,~~ wherein creating the droop in the output signal further comprises[:]

multiplying a sensed current in a feedback loop with a signal inversely proportional to a reference voltage and a signal inversely proportional to a frequency in which the load operates, wherein the reference voltage is reflective of a desired operating voltage of the load.

5. (Currently amended) A method of operating a DC/DC converter having an output coupled to a load with two or more modes of operations, the method comprising:

coupling a power source to an input of the DC/DC converter;

creating a droop in an output signal to the load in response in part to a signal from the power source and in response in part to the operating mode of the load such that the droop is substantially symmetrical throughout the operational modes of the DC/DC converter[.]; and

~~The method of claim 1,~~ wherein creating the droop in the output signal further comprises[:]

multiplying a sensed current in a feedback loop with a signal that is inversely proportional to a reference voltage squared, wherein the reference voltage is reflective of a desired operating voltage of the load.

6. (Currently amended) A method of operating a DC/DC converter having an output coupled to a load with two or more modes of operations, the method comprising:

coupling a power source to an input of the DC/DC converter;

creating a droop in an output signal to the load in response in part to a signal from the power source and in response in part to the operating mode of the load such that the droop is substantially symmetrical throughout the operational modes of the DC/DC converter[.]; and

~~The method of claim 1,~~ wherein creating the droop in the output signal further comprises[:]

controlling a gain of a buffer amplifier in a feedback loop with a frequency signal proportional to the frequency in which the load operates.

7. (original) The method of claim 6, wherein the frequency signal is derived from a reference voltage, wherein the reference voltage is associated with a desired operating voltage of the load.

8-11 (canceled).

REMARKS

Applicant has reviewed the Advisory Action mailed February 1, 2005 and the Final Office Action mailed on October 18, 2004 as well as the art cited. Claims 1, 8-11 have been canceled. Claims 2-7 have been amended. Claims 2-7 are pending in this application.

Claim Objection

Claims 1 and 8-11 were rejected. Applicant has canceled claims 1 and 8-11.

Claims 2-7 were objected to in the Advisory Action. The Applicant has amended claims 2-7 to includes the all the limitations in there respective independent claim and any intervening claim. As such, the Applicant respectfully requests the withdrawal of the rejection of claim 2-7.

The Applicant has merely made the above amendments to get the application to issue into a patent. Accordingly, the Applicant retains the right to submit a continuation application, while this application is pending, that includes claims having a scope that is the same or similar to those claims originally filed in the present application.

Double Patenting Rejection

As indicated by the Examiner in the Advisory Action, the Applicant has overcome the Double Patenting rejection with regard to claims 1-9 and 11.

CONCLUSION

Applicant respectfully submits that Claims 2-7 are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at 612-455-1690.

Respectfully submitted,

Date: 2-28-05

Scott Lundberg
Reg. No. 41,958

Attorneys for Applicant
Fogg and Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339
T – (612) 332-4720
F – (612) 332-4731

Applicant(s)	Volodymyr A.Muratov
Serial No.	10/668,752
Filing Date	September 23, 2003
Group Art Unit	2838
Examiner Name	Younghuie J. Han
Facsimile No.	703-872-9306
Confirmation No.	1792
Attorney Docket No.	125.067US02

FACSIMILE TRANSMITTAL FORM

Title: METHODS TO CONTROL THE DROOP WHEN POWERING DUAL MODE PROCESSORS AND ASSOCIATED CIRCUITS

TOTAL PAGES: 7 pgs. (including cover sheet)
TO CENTRAL FAX – (703) 872-9306
Attention: Examiner Younghuie J. Han, Art Unit 2838

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Enclosures

The following document is enclosed:

X An Amendment and Response Under 37 C.F.R. 1.116 (6 pgs.).

Please charge any additional fees or credit any overpayments to Deposit Account No. 502432.

Submitted By

Name	Scott V. Lundberg	Reg. No.	47,958	Telephone	(612) 332-4720
Signature				Date	February 28, 2005

Attorneys for Applicant
Fogg & Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339
T: 612-332-4720
F: 612-332-4731

CUSTOMER NUMBER: 34206

Certificate of Transmission

I certify that this paper, and the above-identified documents, are being transmitted by facsimile to, Examiner Younghuie J. Han, Group Art Unit 2838 (Facsimile No. 703-872-9306) of the United States Patent and Trademark Office on February 28, 2005.

Name	Elizabeth A. Bauer	Signature	Elizabeth A. Bauer

venient for use in the processor voltage-regulating module. Therefore, a further converter circuit **600** is presented in the FIG. **10**. There a gain control signal proportional to the processor clock frequency in circuit **500** is substituted by the signal **48** derived from the reference V_{DAC} voltage. For known dual-mode processors a reduction in power consumption is usually done with approximately equal scaling of the voltage and the operating frequency. Because of that, some error will be acceptable for practical implementations.

Converter **600** illustrates the implementation of the new method to control the droop when powering the dual mode processors. The DAC **40** receives the code associated with the desired processor operating voltage and sets the reference voltage on its output. The reference voltage V_{DAC} is boosted by the buffer amplifier **42** (BA), which has a variable gain. The level of the offset is programmed by the gain of the buffer amplifier **42**. The same reference signal controls the gain of the buffer amplifier. This forces the level of the initial offset to be proportional to reference voltage squared. The sensed current signal I_{CS} is proportional to the load current I_O and can be either inductor current, switch current, or diode (or synchronous switch) current. I_{CS} is scaled by the factor of gain G_i. This current creates a voltage drop across the resistor **R1**. At the input of the voltage-loop error amplifier, this voltage drop is summed with the voltage feedback signal. As a result, the output voltage of the converter is now inversely proportional to the load current and is in high degree symmetrically positioned along the half-load current.

The output characteristic of the converter, which employs this embodiment of the invention, is described by the generic equation (15), where V_{offset} is determined by the following equation.

$$V_{offset} = \frac{V_{DACi}}{\left(\frac{2-\Delta}{\Delta}\right) \times K_V \times \frac{V_{DACf}}{V_{DACi}} + 1}, \tag{18}$$

$$\text{Where } K_V = \frac{F_{CPU\,max.i} \times V_{DACi}}{F_{CPU\,max.f} \times V_{DACf}}.$$

Table 7 illustrates how this embodiment of the new voltage positioning method provides a converter output with characteristics that are symmetrically centered in both operating modes. This assures the processor power specifications will not be violated in any operation mode.

TABLE 7

		V(o)	V(Imax)	Vnom	+□(mv)	−□(mv)
Droop Tuned to Perf. Mode	Performance Mode	1.640	1.560	1.60	+40	−40
	Battery Mode	1.379	1.321	1.35	+29	−29
Tuned to Battery Mode	Performance Mode	1.641	1.559	1.60	+41	−41
	Battery Mode	1.378	1.322	1.35	+28	−28

The gain setting signal **48** is generated by a decoder circuit **810**. With reference to FIG. **11** the gain of the buffer amplifier **42** is controlled by the VID code that sets the desired value of the processor operating voltage. The gain of the buffer amplifier **42** is defined as G_{BA}=**R3**/**R2**+1. Resistor **R2** is made of the chain of the resistors that are connected to the drains of the switches **820**(n). The VID code is decoded by the decoder **810** connected between VID inputs and the switch gates. The values of the resistors in the resistive chain **R2** are chosen accordingly to the VID code so the desired gain is set. The initial offset voltage programmed by this circuit complies with the following equation.

$$\frac{\Delta_i}{2} = \frac{1}{\left(\frac{2-\Delta 1}{\Delta 1}\right) \times K_V \times \frac{V_{DACf}}{V_{DACi}} + 1} = G_{BA} = \frac{R3}{R2} + 1 \tag{19}$$

Where: Δ_i is a current value of a droop measured as a fraction of the current value of the VDACi setting at the calibration point. The calibration point VDACi could be the highest or the lowest reference voltage, or any other reference voltage from the variety of values programmed by the VID code. Because the described method to control droop affects only the reference voltage of the regulator, it can be implemented in the regulators of both switching and linear nature.

In addition to conserving power in all operational states, utilizing this voltage positioning method may enable processor manufacturers to specify reduced voltage tolerances for their dual mode processor. This reduced voltage tolerance may translate to improved yield characteristics and hence lower manufacturing costs.

In addition to the embodiments described above, others skilled in the art may adapt the invention for use in other droop generating circuits. The circuit of FIG. **1** is just one example of a droop generating DC/DC converter. For example, linear regulator or hysteretic PWM controller may also the output voltage droop and those circuits can be modified to use the steps and structures of the invention.

What is claimed is:

1. A method of operating a DC/DC converter having an output coupled to a load with two or more modes of operations, the method comprising:

coupling a power source to an input of the DC/DC converter;

creating a droop in an output signal to the load in response in part to a signal from the power source and in response in part to the operating mode of the load such that the droop is substantially symmetrical throughout the operational modes of the DC/DC converter; and wherein creating the droop in the output signal further comprises:

multiplying a sensed current in a feedback loop with a signal that is inversely proportional to a frequency of the load.

2. A method of operating a DC/DC converter having an output coupled to a load with two or more modes of operations, the method comprising:

coupling a power source to an input of the DC/DC converter;

creating a droop in an output signal to the load in response in part to a signal from the power source and in response in part to the operating mode of the load such that the droop is substantially symmetrical throughout the operational modes of the DC/DC converter; and wherein creating the droop in the output signal further comprises

multiplying a sensed current in a feedback loop with a signal that is inversely proportional to a reference voltage, wherein the reference voltage is associated with a desired operating voltage of the load.

3. A method of operating a DC/DC converter having an output coupled to a load with two or more modes of operations, the method comprising:

coupling a power source to an input of the DC/DC converter;

creating a droop in an output signal to the load in response in part to a signal from the power source and in response in part to the operating mode of the load such that the droop is substantially symmetrical throughout the operational modes of the DC/DC converter; and wherein creating the droop in the output signal further cornprises

multiplying a sensed current in a feedback loop with a signal inversely proportional to a reference voltage and a signal inversely proportional to a frequency in which the load operates, wherein the reference voltage is reflective of a desired operating voltage of the loud.

4. A method of operating a DC/DC converter having an output coupled to a load with two or more modes of operations, the method comprising:

coupling a power source to an input of the DC/DC converter;

creating a droop in an output signal to the load in response in part to a signal from the power source and in response in part to the operating mode of the load such that the droop is substantially symmetrical throughout the operational modes of the DC/DC converter; and wherein creating the droop in the output signal further comprises

multiplying a sensed current in a feedback loop with a signal that is inversely proportional to a reference voltage squared, wherein the reference voltage is reflective of a desired operating voltage of the load.

5. A method of operating a DC/DC converter having an output coupled to a load with two or more modes of operations, the method comprising:

coupling a power source to an input of the DC/DC converter;

creating a droop in an output signal to the load in response in part to a signal from the power source and in response in part to the operating mode of the load such that the droop is substantially symmetrical throughout the operational modes of the DC/DC converter; and wherein creating the droop in the output signal further comprises

controlling a gain of a buffer amplifier in a feedback loop with a frequency signal proportional to the frequency in which the load operates.

6. The method of claim **5**, wherein the frequency signal is derived from a reference voltage, wherein the reference voltage is associated with a desired operating voltage of the loud.

* * * * *